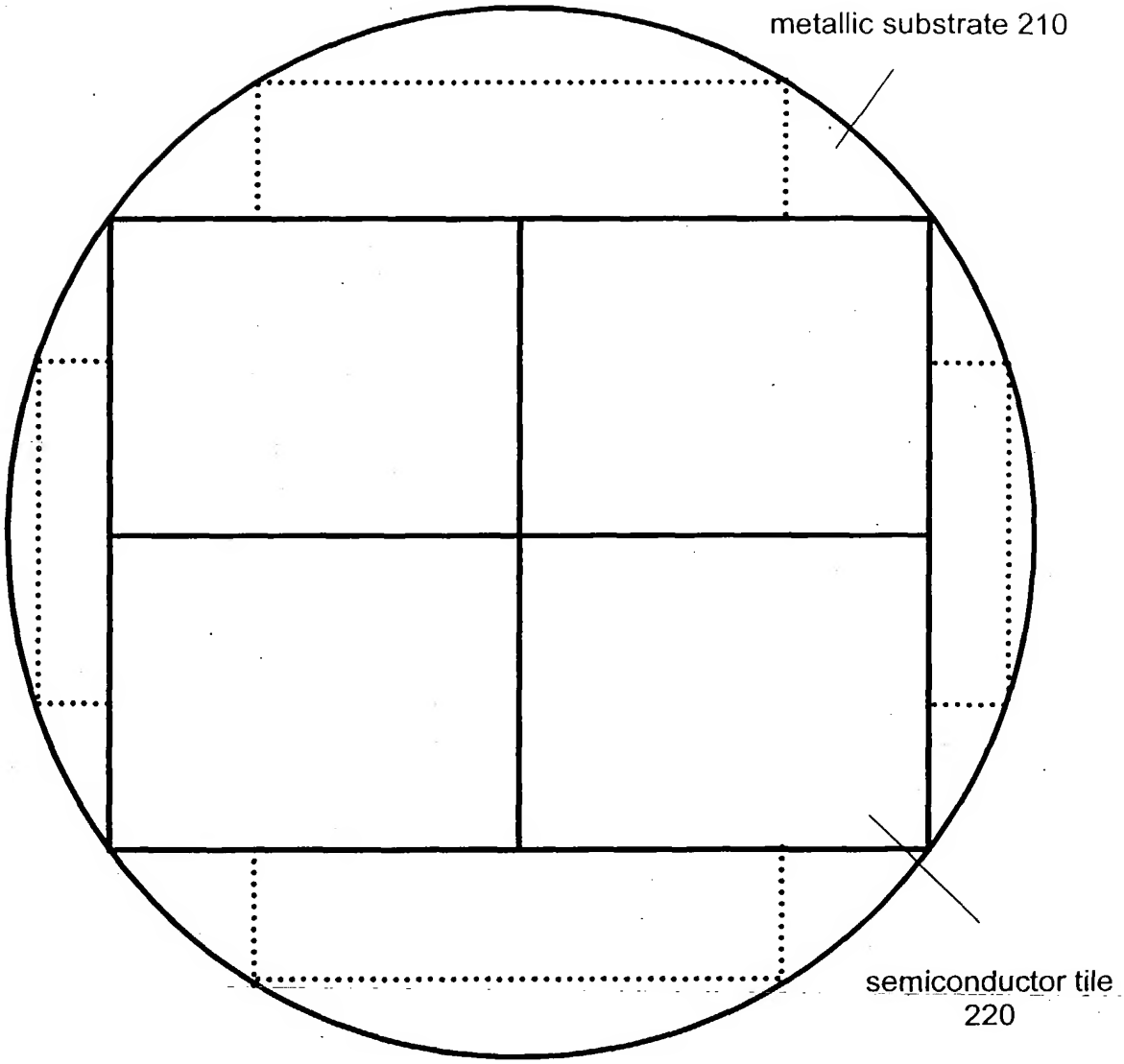


FIG. 1

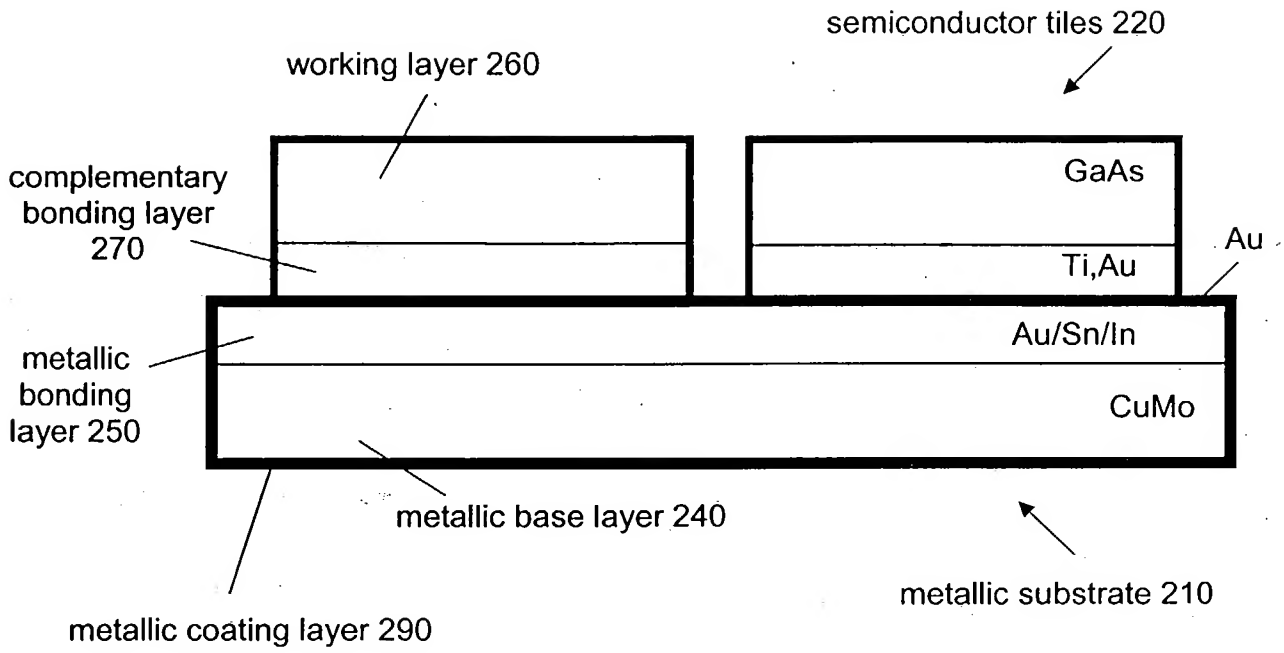

semiconductor tiles 220
working layer 260
complementary bonding layer 270
GaAs
Ti,Au
Au
Au/Sn/In
metallic bonding layer 250
CuMo
metallic base layer 240
metallic substrate 210
metallic coating layer 290

FIG. 2

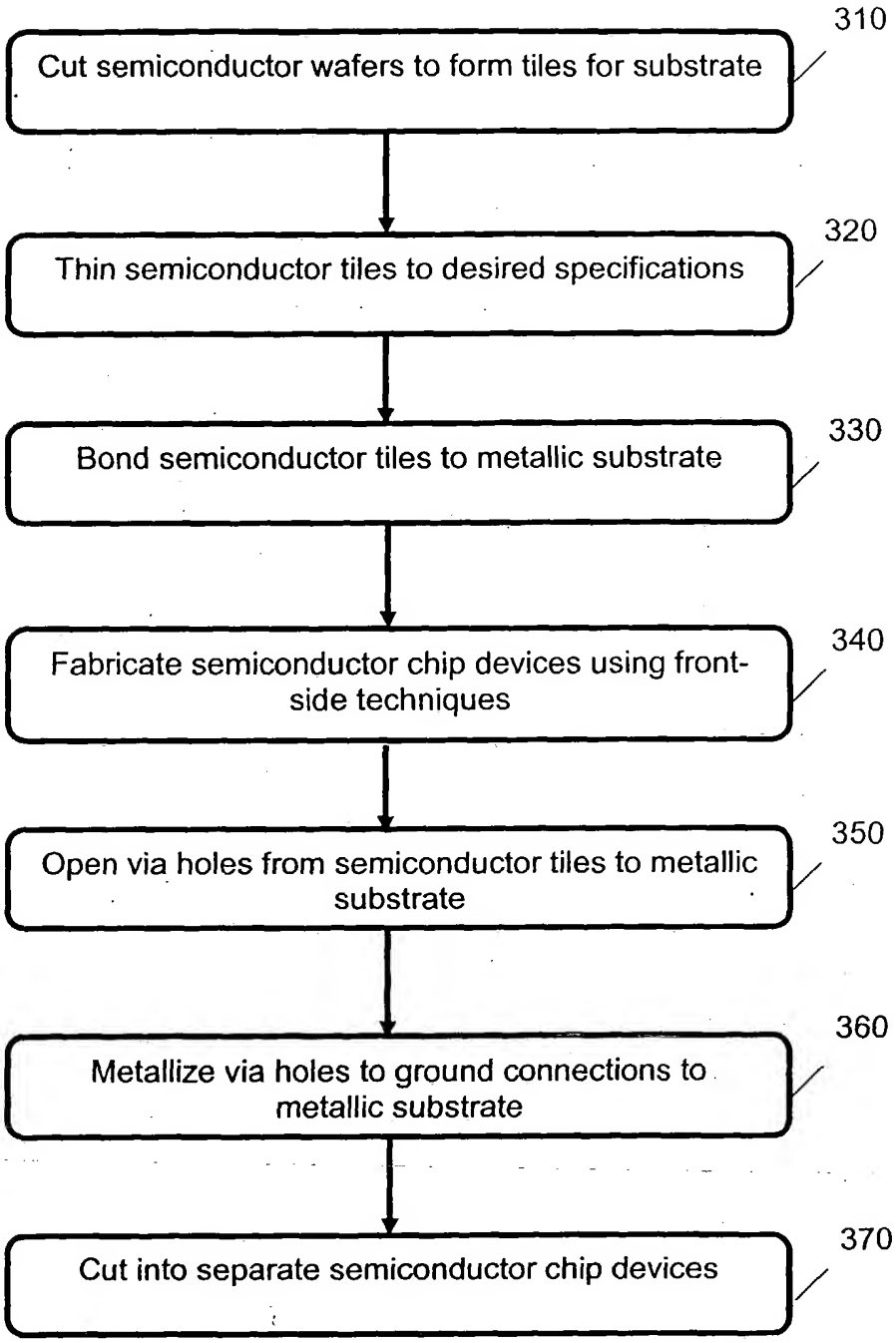
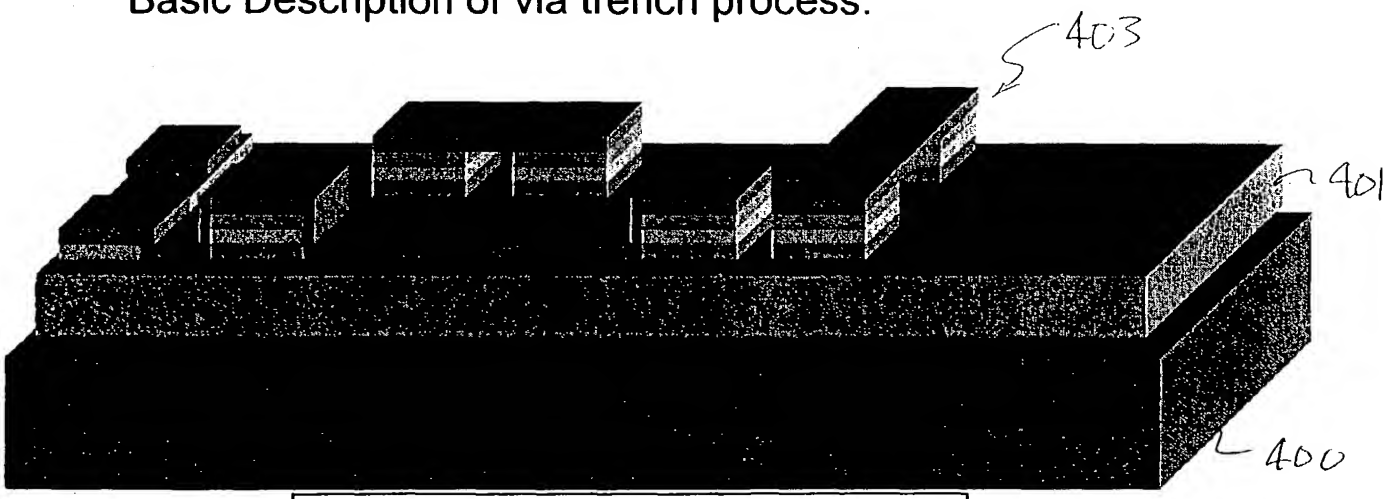

310
Cut semiconductor wafers to form tiles for substrate
320
Thin semiconductor tiles to desired specifications
330
Bond semiconductor tiles to metallic substrate
340
Fabricate semiconductor chip devices using front-side techniques
350
Open via holes from semiconductor tiles to metallic substrate
360
Metallize via holes to ground connections to metallic substrate
370
Cut into separate semiconductor chip devices

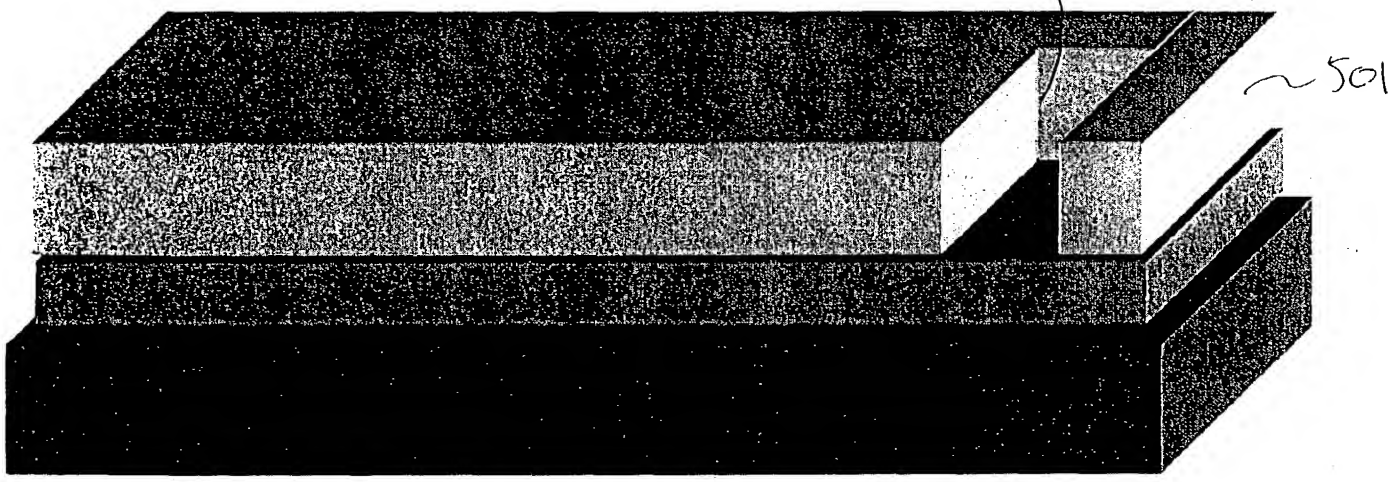
FIG. 3

Basic Description of via trench process:



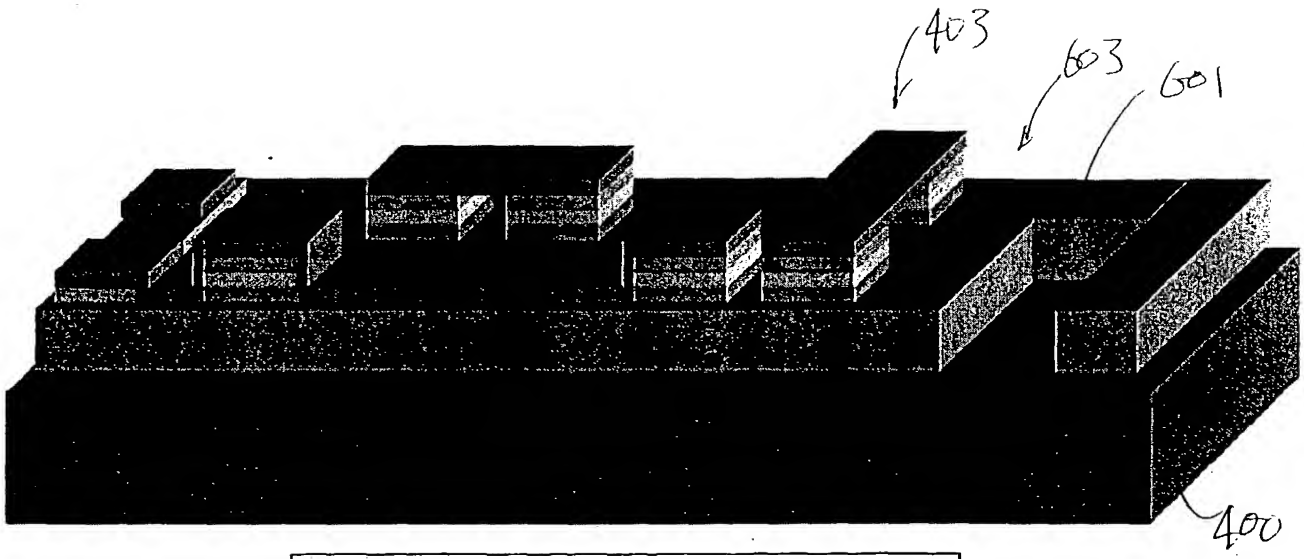
Front side processing complete except for via holes

FIG. 4



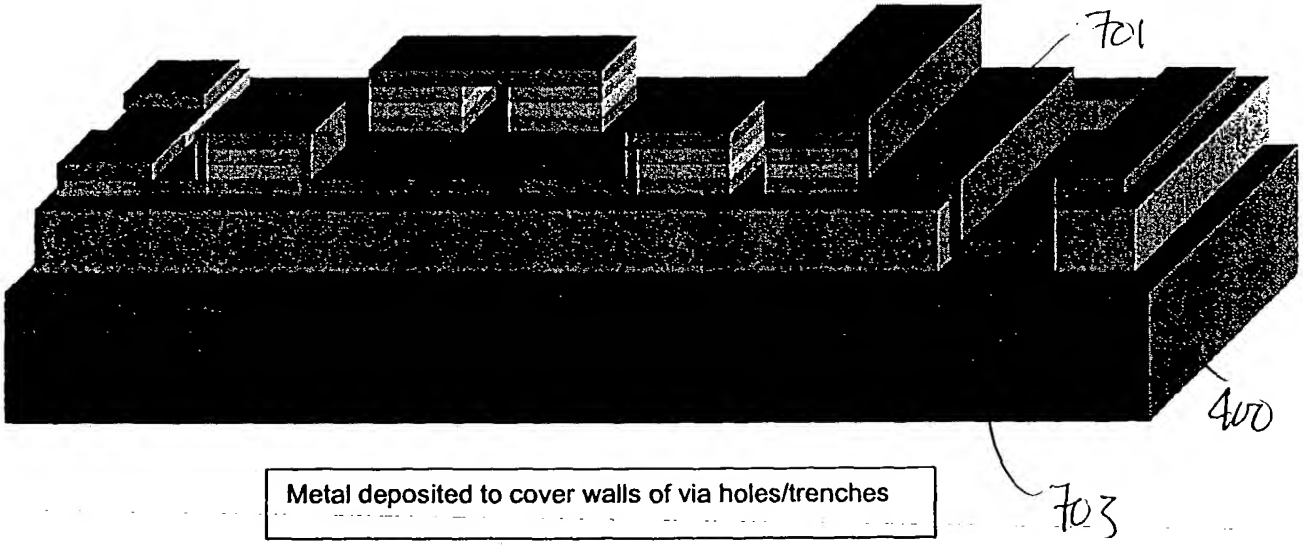
Wafer covered with photoresist. PR exposed using standard front-side mask alignment techniques and developed to expose GaAs wafer at certain locations

FIG. 5



Via holes/trenches etched using standard etching techniques such as reactive ion etching. PR removed.

FIG. 6



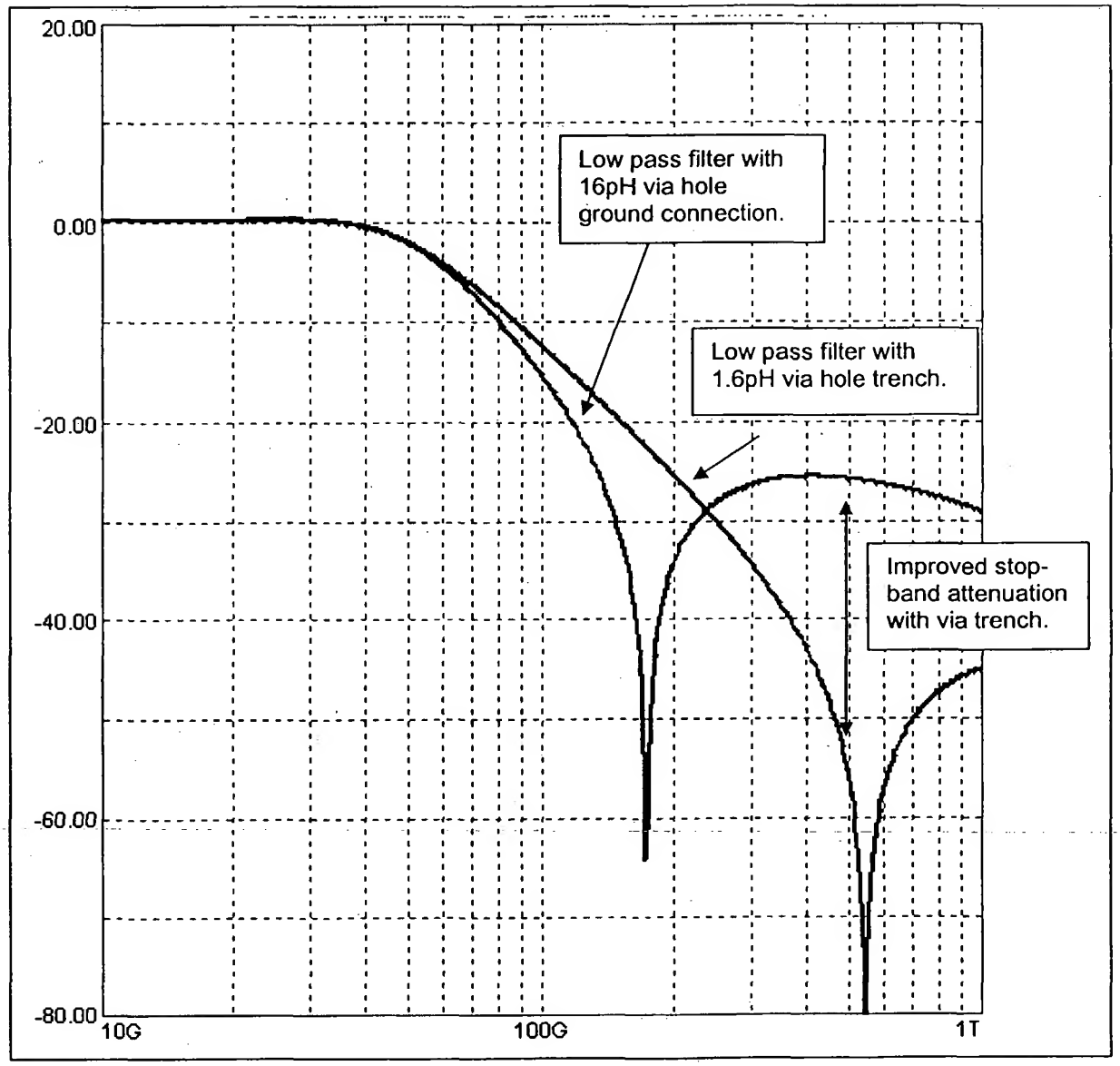
Metal deposited to cover walls of via holes/trenches

FIG. 7

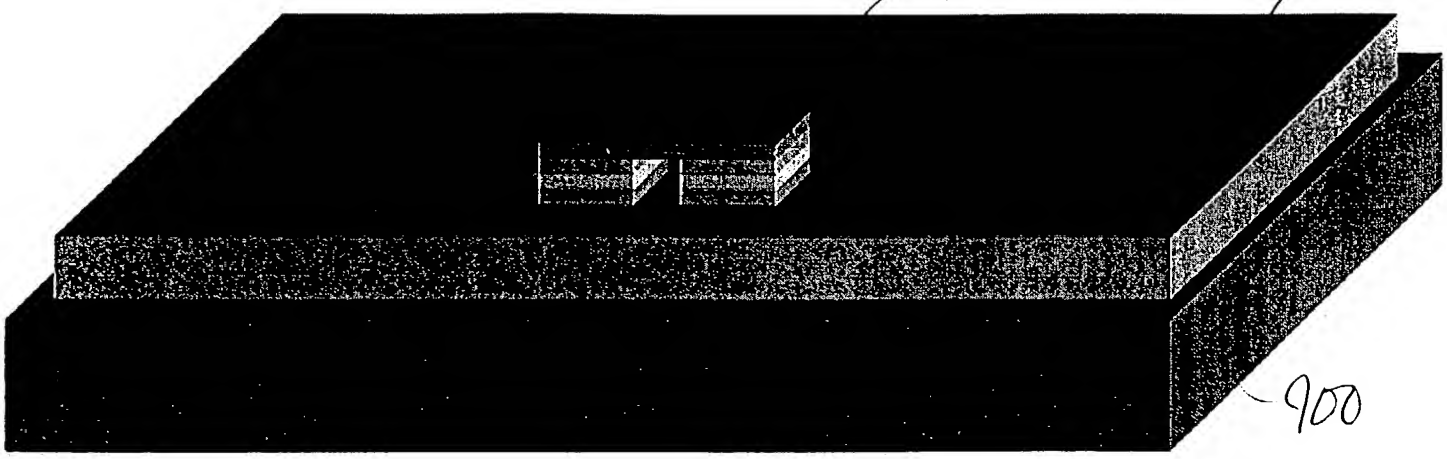
Notes on via hole parameters:

Standard via holes are round with diameters in range 50 – 100 microns. They have between 8 and 16pH of inductance. By increasing the perimeter of the via hole eg so that it forms a trench, a much lower indcutance eg 1pH can be obtained . This lower inductance is of benefit in circuits such as amplifiers and filters which require low impedance ground connections at very high frequencies.

FIG. 8

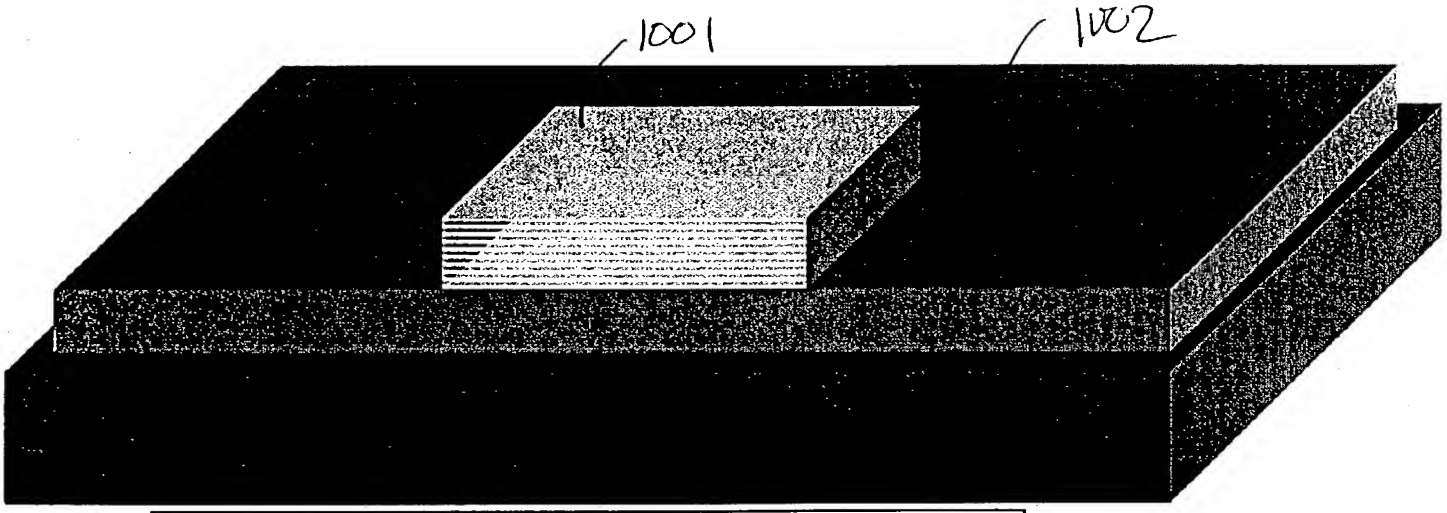


Description of "Metal Box" Feature:



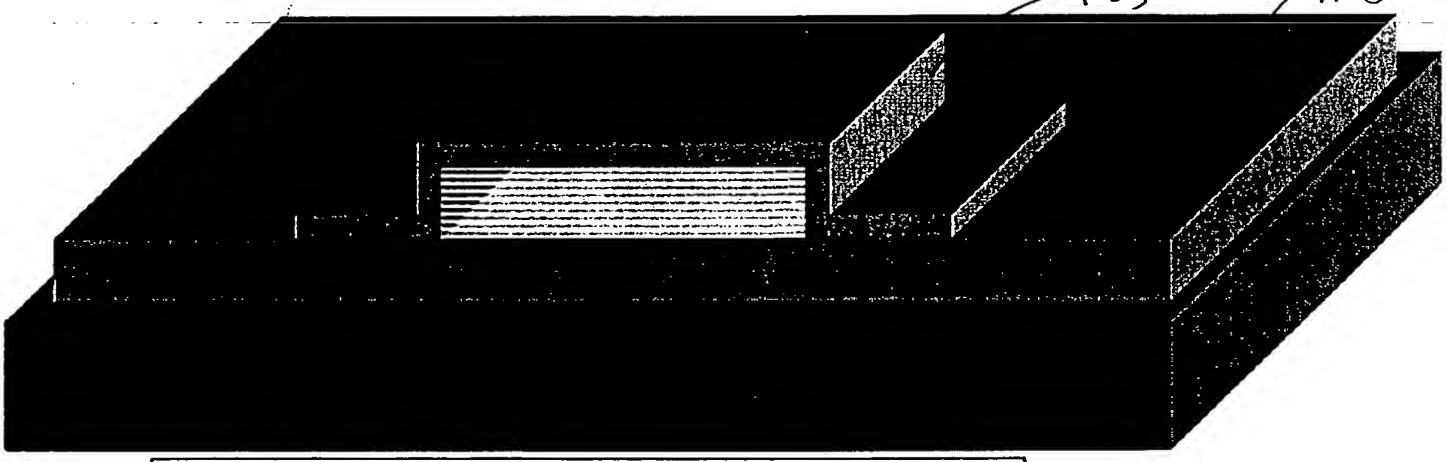
GaAs chip bonded to CuMo substrate with active circuitry on top.

FIG. 9



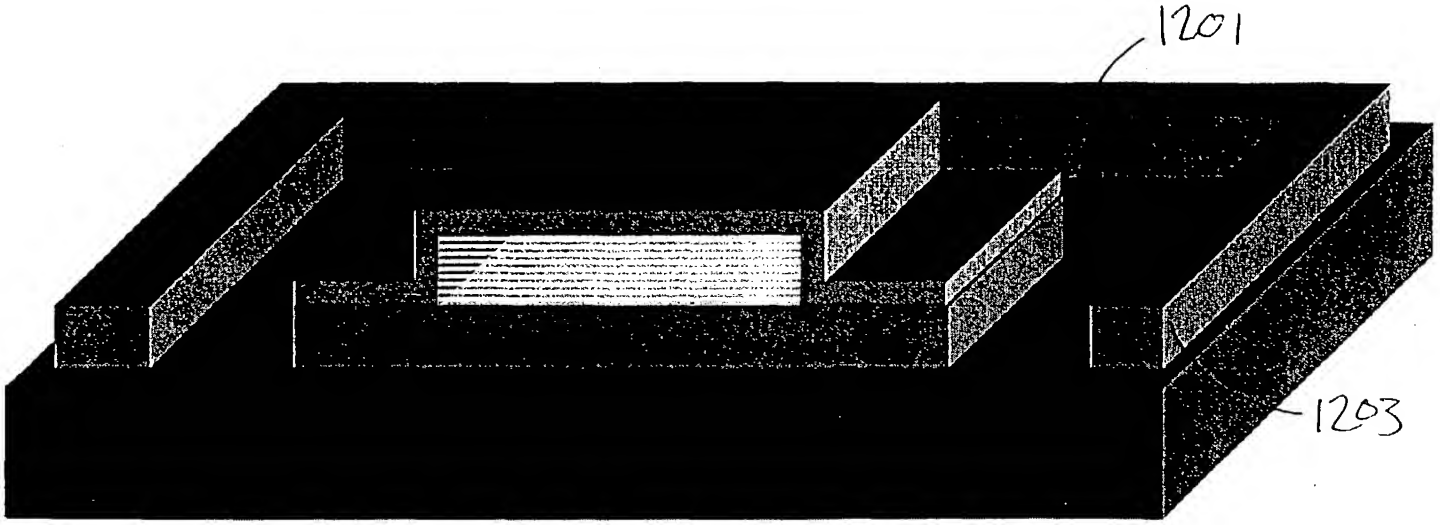
Wafer covered with polymer such as polyimide. Polymer then patterned by photolithography to cover only certain areas of wafer.

FIG. 10



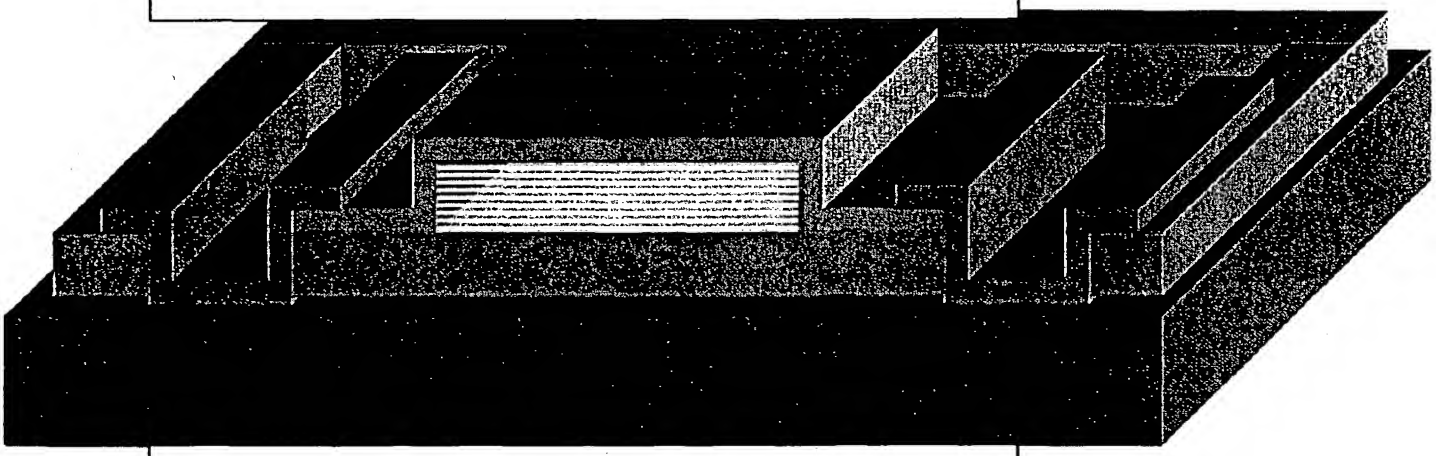
Wafer cov red with metal. Metal is patterned to only cover polymer.

FIG. 11



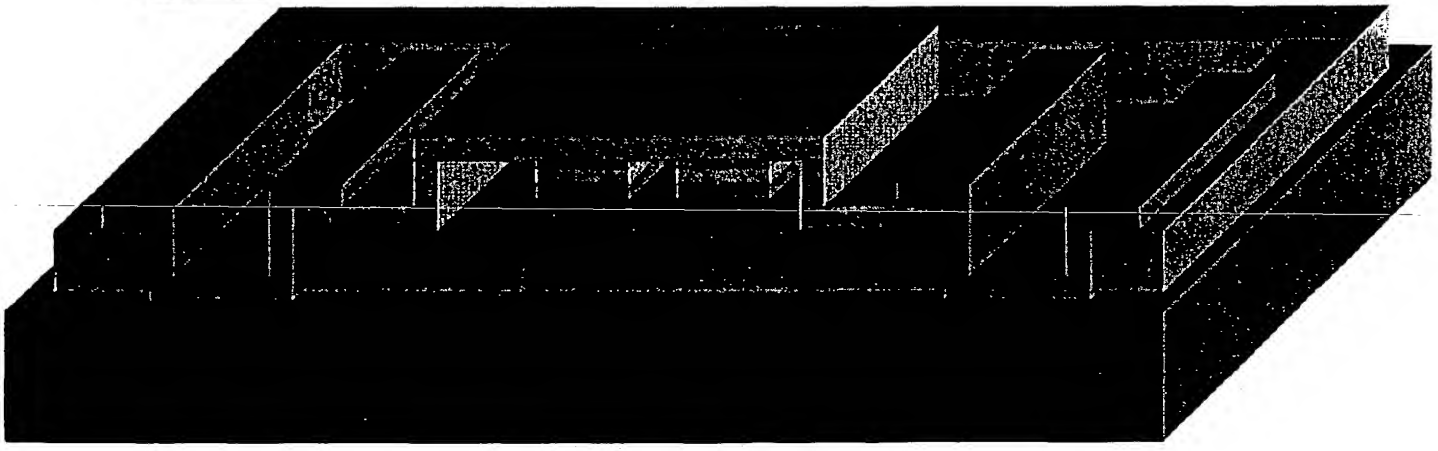
Via hole trench is etched through GaAs surrounding area of active circuitry.

FIG. 12



Metal deposited to cover via trench walls, thereby forming walls of screened box.

FIG. 13



Optionally: polymer is disolved from under metal "air bridge" to reduce capacitance to active circuitry..

FIG. 14

Notes:

Although the diagrams above show the box "top" being formed first, the walls ie trenches could be formed first with the top added later.

Side view of "box":

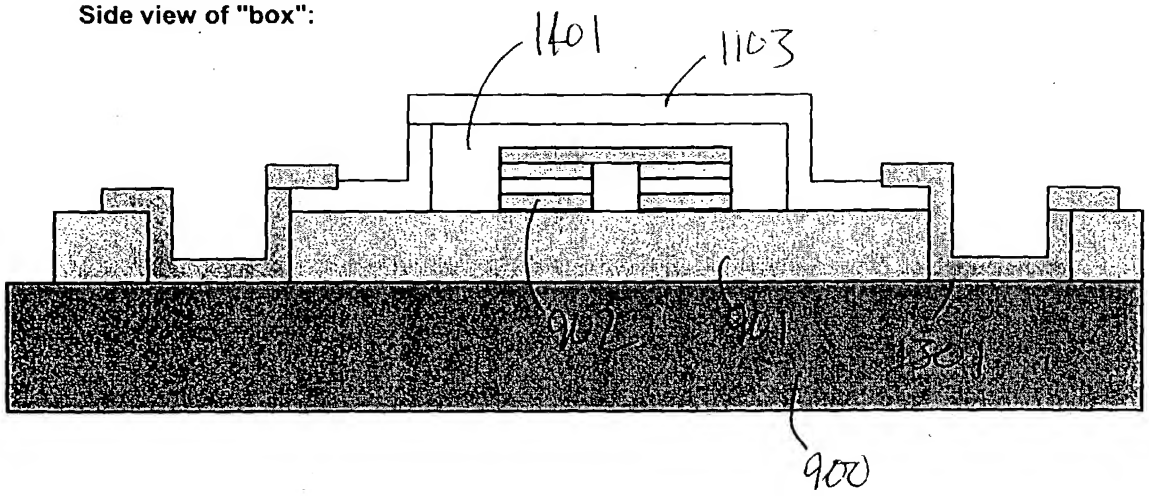


FIG. 15